A2 Concl'd.

deposited to be planarized to the top surface of the SiO_2 film 9 using the chemical mechanical polishing (CMP) method or the etch back. At this time, the lamination of the thin sacrificial oxide film 11 is used for separating the polycrystalline silicon 10 from the silicon substrate 1.

IN THE CLAIMS:

Please amend claims 11 and 12:

A3

11. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising the steps of:

selectively forming an oxide film on said semiconductor substrate;

using the selectively formed oxide films as a mask to carry out etching to form a groove;

laminating a semiconductor layer in said groove to polish top surfaces of said oxide film and said semiconductor film, and thereafter, removing said oxide film;

using said semiconductor film as a mask to diffuse an impurity in the surface of said semiconductor substrate to form a grooved impurity diffusion region including the bottom of said groove;

arranging a gate insulator film of a high dielectric film

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A3 Cont'd

in a groove portion of said grooved impurity diffusion region so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said impurity diffusion region other than said groove portion; and

forming a gate electrode on the top surface of said gate insulator film.

12. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising the steps of:

selectively forming a semiconductor layer on said semiconductor substrate;

using the selectively formed semiconductor layer as a mask to diffuse an impurity in a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region elevated from a channel plane which is formed on the surface of the masked semiconductor substrate;

forming an oxide film on the side of the surface of said elevated impurity diffusion region to use said semiconductor

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.3 Fr. Cont'd.

layer as a stopper to polish a surface of said oxide film, and thereafter, removing said semiconductor layer;

forming a gate insulator film of a high dielectric film in a region bordering elevated impurity diffusion region and said oxide film so that a top surface of said gate insulator film is arranged farther from said substrate than an interface between said impurity diffusion region and said oxide film; and

forming a gate electrode on the top surface of said gate insulator film.

REMARKS

The requested Amendment is fully supported by the Specification and drawings, will not require an additional search, and does not raise new issues. Therefore, applicant respectfully requests that this Preliminary Amendment be entered and the requested changes made. No new matter enteres by this amendment.

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